

Course Description

Use the ISE® software tools to implement a design and gain a firm understanding of the Xilinx FPGA architecture. Learn the best design practices from the pros and understand the subtleties of the Xilinx design flow.

This course covers ISE software 12.1 features, such as the Architecture Wizard, I/O Planner, and the Constraints Editor. Other topics include FPGA architecture, good design practices, understanding report contents, and global timing constraints.

For more emphasis on improving the overall design performance, take the follow-up course *Designing for Performance*, which builds on the basic principles covered in this course.

Level – FPGA 2

Course Duration – 1 day

Price – \$700 or 7 training credits

Course Part Number – FPGA23000-12-ILT

Who Should Attend? – Digital designers who have a working knowledge of HDL (VHDL or Verilog) and who are new to Xilinx FPGAs

Recommended RELs

- Architecture Wizard and I/O Planning REL*

Prerequisites

- Working HDL knowledge (VHDL or Verilog)
- Digital design experience

Other Optional RELs

- Basic HDL Coding Techniques REL* (parts 1 and 2)
- Virtex-6 and Spartan-6 FPGA HDL Coding Techniques REL* (parts 1 and 2)

Software Tools

- Xilinx ISE Design Suite: Logic or System Edition 12.1

Hardware

- Architecture: Spartan®-6 FPGA**
- Demo board: Spartan-6 FPGA SP605 board**

* Go to www.xilinx.com/education and click the Recorded e-Learning link to view these RELs.

** This course focuses on the Spartan-6 architecture. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Take advantage of the primary features of the Spartan-6 FPGA
- Use the Xilinx Project Navigator to implement and simulate an FPGA design
- Read reports and determine whether your design goals were met
- Use the Clocking Wizard to create DCM instantiations
- Use the I/O Planner to make good pin assignments
- Use the Xilinx Constraints Editor to enter global timing constraints

Course Outline

- Course Agenda
- Basic FPGA Architecture
- Xilinx Tool Flow
- Lab 1:** Xilinx Tool Flow
- Reading Reports
- Lab 2:** Clocking Wizard and Pin Assignment

- Lab 3:** Pre-Assigning I/O Pins Using the PlanAhead Tool
- Global Timing Constraints
- Lab 4:** Global Timing Constraints
- Synchronous Design Techniques
- Course Summary

Lab Descriptions

- Lab 1:** Xilinx Tool Flow – Create a new project in the ISE Project Navigator and use the ISE Simulator to perform a behavioral simulation. Implement the design using default software options and download to a Spartan-6 FPGA SP605 evaluation board.
- Lab 2:** Clocking Wizard and Pin Assignment – Use the Clocking Wizard to customize a DCM and incorporate your clocking resources into your design. Use the PlanAhead™ tool to assign pin locations and implement the design using the Project Navigator in the ISE software.
- Lab 3:** Pre-Assigning I/O Pins Using the PlanAhead Tool – This lab introduces the basics of making good I/O pin assignments with the PlanAhead software. Use the Design Rule Checker to follow the I/O banking rules.
- Lab 4:** Global Timing Constraints – Enter global timing constraints with the Xilinx Constraints Editor. Review the Post-Map Static Timing Report to verify that the timing constraints are realistic. Use the Post-Place & Route Static Timing Report to determine the delay of the longest constrained path for each timing constraint.

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Please send inquiries to info@vaitechnology.com, or contact the registrar at (317) 570-0707.

