

Course Description

Learn to manage design performance, plan an I/O pin layout, and implement by using the PlanAhead™ software tool. Topics include: a tool overview, running a Design Rule Check (DRC) and Simultaneous Switching Noise (SSN) analysis of pin assignments, design and timing analysis, creating cores, and completing synthesis and implementation with the PlanAhead tool.

Note: The hands-on labs provided within this course are identical to the tutorials that are packaged with the PlanAhead tool. This course is supplemented with instructor-led presentations and a demonstration.

Level – FPGA 1

Course Duration – 1 day

Price – \$700 or 7 training credits

Course Part Number – FPGA12000-12-ILT

Who Should Attend? – FPGA designers, system architects, and system engineers who are interested in analyzing and driving the physical implementation of their designs to maximize performance and capacity.

Prerequisites

- *Essentials of FPGA Design* or equivalent knowledge of the FPGA architecture and the Xilinx ISE® software flow
- *Designing for Performance* recommended

Software Tools

- Xilinx ISE Design Suite: Logic or System Edition 12.1

Hardware

- Architecture: Virtex®-6 FPGA*
- Demo board: None*

* This course focuses on the Virtex-6 architecture. Check with your local Authorized Training Provider for specifics or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Use the PlanAhead tool features and benefits
- Import designs into the PlanAhead tool project environment
- Assign I/O pins and clock logic
- Run DRC and SSN noise analysis
- Integrate IP with the PlanAhead tool
- Import HDL sources, elaborate, and analyze the RTL netlist
- Implement the design with different implementation strategies
- Analyze design statistics and timing
- Use the PlanAhead tool integrated with the ISE tool Project Navigator environment

Course Outline

- PlanAhead Tool Benefits and Features Overview
- PlanAhead Tool Project Manager
 - **Lab 1:** Getting Started with the PlanAhead Tool
- I/O Pin Planning
 - **Lab 2:** Assigning I/O Pins
- CORE Generator Tool Integration
 - **Lab 3:** CORE Generator Tool Integration
- Project Navigator Integration
- Introduction to the *Advanced Design with the PlanAhead Analysis and Design Tool* Course

Lab Descriptions

Note: All labs within this course are also available as self-guided tutorials, which are packaged with the PlanAhead tool.

- **Lab 1:** Getting Started with the PlanAhead Tool – Illustrates the steps you take to import an RTL design into the PlanAhead tool so that you can synthesize, add timing constraints, implement, perform timing analysis, and generate a bitstream. Also introduces the PlanAhead tool environment and views.
- **Lab 2:** Assigning I/O Pins – Introduces the PlanAhead tool's pin planning environment for performing I/O pin assignment. You will create a project, import and export I/O ports lists, create I/O ports and interfaces, run a DRC and SSN noise analysis, make clock logic placement, and make pin assignments.
- **Lab 3:** CORE Generator Tool Integration – Illustrates the integration of the CORE Generator tool with the PlanAhead software. You will customize and integrate a core, explore the IP Catalog, and view the generated core with the Schematic viewer.

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Please send inquiries to info@vaitechnology.com, or contact the registrar at (317) 570-0707.

