

### Course Description

Are you interested in learning how to effectively utilize Virtex®-6 FPGA architectural resources? This course supports both experienced and less experienced FPGA designers who have already completed the *Essentials of FPGA Design* course. This course focuses on understanding as well as how to properly design for the primary resources found in this popular device family.

Topics covered include device overviews, CLB construction, MMCM clocking resources, global, regional and I/O clocking techniques, memory, FIFO resources, DSP, and source-synchronous resources. Soft memory controller support and the dedicated hardware resources available in each of the sub-families (EMAC, PCI Express® technology, and GTP transceivers) are also introduced.

This course also includes a detailed discussion about proper HDL coding techniques that enables designers to avoid common mistakes and get the most out of their FPGA. A combination of modules and labs allow for practical hands-on application of the principles taught.

**Level** – FPGA 3

**Course Duration** – 2 day

**Price** – \$1400 or 14 training credits

**Course Part Number** – V6-21000-11-ILT

**Who Should Attend?** – For those who have taken the *Essentials of FPGA Design* course

**Prerequisites**

- *Essentials of FPGA Design* course
- Intermediate VHDL or Verilog knowledge

**Software Tool**

- Xilinx ISE® Design Suite: Logic or System Edition 11.3

**Hardware**

- Architecture: Virtex-6 FPGA\*
- Demo board: None\*

\* This course focuses on the Virtex-6 architecture. Check with your local Authorized Training Provider for specifics or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe all the functionality of the 6-input LUT and the CLB construction of the Virtex-6 FPGA
- Specify the CLB resources and the available slice configurations for the Virtex-6 FPGA
- Define the block RAM, FIFO, and DSP resources available for the Virtex-6 FPGA
- Properly design for the I/O block and SERDES resources
- Identify the MMCM and clock routing resources included with this family
- Identify the supported soft memory controllers for the Virtex-6 FPGA
- Properly code your HDL to get the most out of the Virtex-6 FPGA
- Describe the additional dedicated hardware for all the Virtex-6 family members

### Course Outline

#### Day 1

- Virtex-6 FPGA Overview
- CLB Architecture
- **Lab 1:** CLB Resources
- Memory Resources
- DSP Resources
- **Lab 2:** DSP Resources

- Basic I/O Resources
- Virtex-6 FPGA I/O Resources
- **Lab 3:** I/O Resources

#### Day 2

- Basic Clocking Resources
- Virtex-6 FPGA Clocking Resources
- **Lab 4:** Clocking Resources
- Memory Controllers
- HDL Coding Techniques
- **Lab 5:** HDL Coding Techniques
- Dedicated Hardware

### Lab Descriptions

- **Lab 1: CLB Resources** – Gain comprehensive experience with the CLB architecture. Synthesize a 32-bit incrementer with terminal count logic and pipelining registers. Verify that the appropriate resources were used with the RTL and technology viewers included with XST. Use the FPGA Editor to inspect the implemented results.
- **Lab 2: DSP Resources** – Using XST, synthesize and implement a 24x17 MAC. Device usage will be verified via the FPGA Editor. Using the CORE Generator™ tool, construct, instantiate, and implement a wide pipelined multiplier. Verify the results with the FPGA Editor.
- **Lab3: I/O Resources** – Using the ISE tools, complete the construction of the transmit SERDES datapath. Explore, through simulation, the behavior of the various blocks. Also use the FPGA Editor to explore the physical resources of the Virtex-6 FPGA tile used for construction of a high-speed interface.
- **Lab 4: Clocking Resources** – Using the Clocking Wizard, build and optimize the appropriate MMCM and clock routing resources. Also instantiate these resources into the design. After the design is implemented, verify hardware usage with the FPGA Editor and explore other aspects of the silicon layout.
- **Lab 5: HDL Coding Techniques** – Using XST, synthesize various components into the design and evaluate the impact that proper HDL coding techniques have on the size and speed of implementation results.

### Register Today

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