

## Course Description

*Advanced FPGA Implementation* tackles the most sophisticated aspects of the ISE® 11.3 design suite and Xilinx hardware. Seven labs provide hands-on experience in this two-day training and cover the Xilinx Synthesis Technology (XST) tools.

This course requires the *Essentials of FPGA Design* and *Designing for Performance* courses as prerequisites. An intermediate knowledge of Verilog or VHDL is strongly recommended as is at least six months of design experience with Xilinx tools and FPGAs. The lecture material in this course covers the ISE 11.3 tools and the Spartan®-6 and Virtex®-6 FPGAs.

#### Level – FPGA 4

**Course Duration** – 2 days

**Price** – \$1400 or 14 training credits

**Course Part Number** – FPGA33000-11-ILT

**Who Should Attend?** – Engineers who seek advanced training in using Xilinx tools to improve FPGA performance and utilization while also increasing productivity

#### Prerequisites

- *Essentials of FPGA Design*
- *Designing for Performance*
- Intermediate knowledge of Verilog or VHDL is strongly recommended
- At least six months of design experience with Xilinx tools and FPGAs

#### Software Tools

- Xilinx ISE Design Suite: Logic or System Edition 11.3

#### Hardware

- Architecture: Spartan-6 and Virtex-6 FPGAs\*
- Demo board: Spartan-6 FPGA SP605 board\*

\* This course focuses on the Spartan-6 and Virtex-6 architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Create and edit a User Constraint File (UCF)
- Identify the I/O timing constraints and design modifications required for source-synchronous and system-synchronous interfaces
- Implement designs via the Tcl command line
- Preserve design results by using SmartGuide™ technology
- Use the PlanAhead™ tool to create area constraints
- Change signals of interest in the ChipScope™ Pro tool for board-level debugging using the FPGA Editor

## Course Outline

- Introduction
- **Lab 1:** Timing Closure Review
- UCF Editing
- **Lab 2:** UCF Editing
- Advanced I/O Timing
- **Lab 3:** Advanced I/O Timing
- Tcl Scripting
- **Lab 4:** Tcl Scripting
- SmartGuide Technology
- **Lab 5:** SmartGuide Technology

- Floorplanning an Effective Layout
- **Lab 6:** Floorplanning
- FPGA Editor: Viewing and Editing a Routed Design
- **Lab 7:** Advanced FPGA Editor

## Lab Descriptions

**Note:** Labs will be based on Xilinx ISE 11.3 software.

- **Lab 1:** Timing Closure Review – Use the Constraints Editor to enter timing constraints.
- **Lab 2:** UCF Editing – Write constraints directly into a UCF file to guide the performance results of implementation.
- **Lab 3:** Advanced I/O Timing – Compose timing constraints for source-synchronous and system-synchronous I/O interfaces. Analyze the timing and determine changes to optimize the interface timing.
- **Lab 4:** Tcl Scripting – Write ISE tool control commands in Tcl script files to create a project and implement the design. Explore how the Tcl interface is integrated with the Project Navigator tool.
- **Lab 5:** SmartGuide Technology – Utilize SmartGuide technology to preserve the timing results from one iteration to the next.
- **Lab 6:** Floorplanning – Implement a design by using floorplanned constraints to improve the timing results over a design without floorplanning.
- **Lab 7:** Advanced FPGA Editor – Use the FPGA Editor to view and edit a design. Rapidly locate and swap signals of interest for ChipScope Pro tool cores.

## Register Today

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