

Course Description

ISE Design Tool Flow provides the overall context and framework for the development cycle of FPGAs. For those uninitiated to FPGA design, this course will arm you with the proper planning techniques, strategy, and FPGA tool flow to get up and designing an FPGA design now.

The flow will take you from behavioral specification to tuning specifications for the FPGA, synthesis, verification, and onto implementation and download. Throughout the design cycle, the various tools within the Project Navigator tool are introduced.

Level – FPGA 1

Course Duration – 1 day

Price – \$700 or 7 training credits

Course Part Number – FPGA16000-12-ILT

Who Should Attend? – Digital designers new to FPGA design who need to learn the FPGA design cycle and the major aspects of the ISE® 12.1 design tools

Prerequisites

- Basic knowledge of the VHDL or Verilog language

Recommended RELs*

- Basic FPGA Architecture: Slice and I/O Resources
- Basic FPGA Architecture: Memory and Clocking Resources

Software Tools

- Xilinx ISE Design Suite: Logic or System Edition 12.1

Hardware

- Architecture: Spartan®-6 and Virtex®-6 FPGAs**
- Demo board: None**

* Go to www.xilinx.com/education and click the View Training Modules link to view these RELs.

** This course focuses on the Spartan-6 and Virtex-6 architectures. Check with your local Authorized Training Provider for specifics or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Outline a complete project planning process
- Create a new Project Navigator project in the ISE software
- Access and modify Xilinx Synthesis Technology (XST) synthesis options
- Assign pin locations using the I/O Planner
- Enter global clock constraints using the Xilinx Constraints Editor
- Simulate a design using the ISim Simulator

Course Outline

- Course Agenda
- Project Planning
- Projects in the Project Navigator
- **Lab 1:** Projects in the Project Navigator
- HDL Synthesis and XST
- **Lab 2:** XST Synthesis Options
- Constraints and the I/O Planner
- **Lab 3:** I/O Pin Planning
- ISim Simulator
- **Lab 4:** ISim Simulator
- Additional Features
- Summary

Lab Descriptions

- **Lab 1:** Projects in the Project Navigator – Gain comprehensive hands-on experience with the HDL flow in the ISE software. Create a new project, add source files, synthesize a design, and use the error navigation feature to fix your HDL code.
- **Lab 2:** Synthesis Options – Modify XST synthesis properties, read synthesis reports to compare the synthesis results with the implemented results, and use the schematic viewer to evaluate the design.
- **Lab 3:** I/O Pin Planning – Review demo board documentation to determine the finished pinout and use PinAhead to assign pin location constraints and pin attributes.
- **Lab 4:** ISim Simulator – Use the project navigator to view an HDL testbench, use the ISim Simulator to run simulation view output waveforms, add signals, and change their viewed format.

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Please send inquiries to info@vaitechnology.com, or contact the registrar at (317) 570-0707.

