

## Course Description

Learn to increase design performance and achieve repeatable results by using the PlanAhead™ software. Topics include: a product overview, synthesis and project tips, design analysis, creating a floorplan, improving performance, experimenting with implementation options, incremental methodology, block-based IP design, and I/O pin assignment.

**Note:** The hands-on labs provided within this course are identical to the tutorials that are packaged with the PlanAhead tool. This course is supplemented with instructor-led presentations and demos.

**Level – FPGA 3****Course Duration – 2 days****Price – \$1400 or 14 training credits****Course Part Number – FPGA11000-11-ILT****Who Should Attend? –** FPGA designers, system architects, and system engineers who are interested in analyzing and driving the physical implementation of their designs to maximize performance and capacity.**Prerequisites**

- *Essentials of FPGA Design* or equivalent knowledge of the FPGA architecture and the Xilinx ISE® software flow
- *Designing for Performance* recommended

**Software Tools**

- Xilinx ISE Design Suite: Logic or System Edition 11.1

**Hardware**

- Architecture: Virtex®-5 FPGA\*
- Demo board: None\*

\*This course focuses on the Virtex-5 architecture. Check with your local Authorized Training Provider for specifics or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Use the PlanAhead tool features and benefits
- Import designs into the PlanAhead tool project environment
- Assign I/O pins and clock logic
- Run the Design Rule Checker (DRC) and WASSO analysis
- Import HDL sources, elaborate and analyze the RTL netlist
- Implement the design with different implementation strategies
- Analyze design statistics, connectivity, timing, placement
- Insert ChipScope™ Pro tool debug cores
- Floorplan the design to improve performance and consistency
- Use the PlanAhead tool integrated with the ISE tool Project Navigator environment

## Course Outline

### Day 1

- PlanAhead Tool Benefits and Features Overview
- **Lab 1:** Getting Started with the PlanAhead Tool
- I/O Pin and Clock Planning
- **Lab 2:** Assigning I/O Pins
- RTL Development and Analysis
- **Lab 3:** RTL Development and Analysis
- Implementing a Design
- **Lab 4:** Implementing with the PlanAhead Tool

### Day 2

- Design Analysis
- **Lab 5:** Design Analysis

- Floorplanning Techniques
- **Lab 6:** Floorplanning
- Debugging with the ChipScope Tool
- **Lab 7:** Debugging with the ChipScope Tool
- Project Navigator Integration with the PlanAhead Tool
- **Lab 8:** Using the PlanAhead Tool with Project Navigator
- Course Summary

## Lab Descriptions

**Note:** All labs within this course are also available as self-guided tutorials, which are packaged with the PlanAhead tool.

- **Lab 1:** Getting Started with the PlanAhead Tool – Illustrates the steps you take to import a synthesized design into the PlanAhead tool so that you can begin floorplanning. Also introduces the PlanAhead tool environment and views.
- **Lab 2:** Assigning I/O Pins – Introduces the PinAhead environment for performing I/O pin assignment. You will create a project, import and export I/O ports lists, create I/O ports and interfaces, and make pin assignments.
- **Lab 3:** RTL Development and Analysis – Provides an overview of the RTL development and analysis environment. You will analyze the RTL logic hierarchy, RTL schematic, RTL resource estimations and run RTL Design Rule Check (DRCs).
- **Lab 4:** Implementing with the PlanAhead Tool – Illustrates a walkthrough of the front-to-back, RTL-to-bitstream design flow. You will run synthesis, import synthesis results, run implementation, and import and analyze the implementation.
- **Lab 5:** Design Analysis – Introduces the pre- and post-implementation design analysis features of the PlanAhead software.
- **Lab 6:** Floorplanning – Provides an introduction to some of the capabilities and benefits of using the PlanAhead tool for designing high-end FPGAs.
- **Lab 7:** Debugging with the ChipScope Tool – Provides an introduction to using the PlanAhead tool for debugging designs with the ChipScope™ Pro cores and tools.
- **Lab 8:** Using the PlanAhead Tool with Project Navigator – Illustrates some of the capabilities and benefits of using the PlanAhead tool integrated within the ISE software Project Navigator environment.

## Register Today

Vai logic, the Authorized Training Provider (ATP) for Indiana, Michigan, Ohio, Kentucky, and western Pennsylvania offers public and private training.

Please visit [www.vaitechnology.com](http://www.vaitechnology.com) for more information, to view schedules, or to register.

Please send inquiries to [info@vaitechnology.com](mailto:info@vaitechnology.com), or contact the registrar at (317) 570-0707.

