

Course Description

Xilinx FPGAs provide a new level of system design capabilities through soft MicroBlaze™ processors, hard PowerPC® processors, and silicon-efficient architectural resources. This course brings experienced FPGA designers up to speed on developing embedded systems using the Embedded Development Kit (EDK). The features and capabilities of the Xilinx MicroBlaze soft processor and the PowerPC 440 processor are also included in the lectures and labs. The hands-on labs provide experience with the development, debugging, and simulation of an embedded system.

Level – EMB HW 3

Course Duration – 2 days

Price – \$1400 or 14 training credits

Course Part Number – EMBD21000-11-ILT

Who Should Attend? – Engineers who are interested in developing embedded systems with the Xilinx MicroBlaze soft processor or IBM PowerPC 440 core using the Embedded Development Kit and a Xilinx FPGA

Prerequisites

- FPGA design experience
- Completion of the *Essentials of FPGA Design* course or equivalent knowledge of Xilinx ISE® software implementation tools
- Basic understanding of C programming
- Some HDL modeling experience

Software Tools

- Xilinx ISE Design Suite: System Edition 11.4
- Mentor Graphics ModelSim simulator

Hardware

- Architecture: Spartan®-6, Virtex®-5, and Virtex-6 FPGAs*
- Demo board: Spartan-3E FPGA 1600E, Spartan-6 FPGA SP605, or Virtex-5 FPGA ML507 board*

* This course focuses on the Spartan-6, Virtex-5, and Virtex-6 architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the various tools that encompass the Xilinx Embedded Development Kit (EDK)
- Rapidly architect an embedded system containing a MicroBlaze or IBM PowerPC processor and Xilinx-supplied CoreConnect bus architecture IP by using the Base System Builder (BSB)
- Utilize the Eclipse-based Software Development Kit (SDK) to develop software applications and debug software
- Create and integrate your own IP into the EDK environment
- Simulate your own custom peripherals with Bus Functional Models (BFMs)

Course Outline

Day 1

- EDK Overview
- Base System Builder
- **Lab 1:** Hardware Construction with the Base System Builder
- Software Development Using SDK
- **Lab 2:** Adding and Downloading Software
- System Buses
- Processor Basics

- Interrupts
- Adding Hardware to an Embedded Design
- **Lab 3:** Adding IP to a Hardware Design

Day 2

- Interfacing to the Processor System
- Designing Your Own Peripheral Using the IPIC Interface
- Installing Your Own Peripheral Using the IPIC Interface
- **Lab 4:** Building Custom IP for an Embedded System – PLB v46 Bus
- Bus Functional Model Simulation
- **Lab 5:** BFM Simulation
- Adding Your Own IP to the Embedded System
- **Lab 6:** Integrating a Custom Peripheral

Lab Descriptions

Both the MicroBlaze and PowerPC 440 processors are supported in the labs. All labs target the Spartan-3E FPGA 1600E, Spartan-6 FPGA SP605, or Virtex-5 FPGA ML507 boards.

- **Lab 1:** Hardware Construction with the Base System Builder – Create an XPS project by using the Base System Builder to develop a basic hardware system and generate a series of netlists for the embedded design.
- **Lab 2:** Adding and Downloading Software – Complete the processes begun in Lab 1 by building the software libraries and applications, generating a bitstream file, merging the application into the bitstream, and downloading to the board.
- **Lab 3:** Adding IP to a Hardware Design – Learn to add IP from the many choices in the IP library. Use the GUI to add a general-purpose I/O module and access internal block RAM directly from the MHS file.
- **Lab 4:** Building Custom IP for an Embedded System – Create and add custom IP (IPIC interface) to your design by using the Create or Import Peripheral Wizard.
- **Lab 5:** BFM Simulation – Use the ModelSim simulator to perform Bus Functional Model simulation to verify functionality of the LCD bus peripheral added in the preceding lab.
- **Lab 6:** Integrating a Custom Peripheral – Put it all together: add custom IP to the processor system, then integrate the processor sub-system with other logic in the design.

Register Today

Vai logic, the Authorized Training Provider (ATP) for Indiana, Michigan, Ohio, Kentucky, and western Pennsylvania offers public and private training.

Please visit www.vaitechnology.com for more information, to view schedules, or to register.

Please send inquiries to info@vaitechnology.com, or contact the registrar at (317) 570-0707.

